Transparent Electronics Based on Transfer Printed Aligned Carbon Nanotubes on Rigid and Flexible Substrates

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ABSTRACT We report high-performance fully transparent thin-film transistors (TTFTs) on both rigid and flexible substrates with transfer printed aligned nanotubes as the active channel and indium—tin oxide as the source, drain, and gate electrodes. Such transistors have been fabricated through low-temperature processing, which allowed device fabrication even on flexible substrates. Transparent transistors with high effective mobilities (~1300 $cm^2 V^{-1} s^{-1}$) were first demonstrated on glass substrates *via* engineering of the source and drain contacts, and high on/off ratio (3×10^4) was achieved using electrical breakdown. In addition, flexible TTFTs with good transparency were also fabricated and successfully operated under bending up to 120°. All of the devices showed good transparency (~80% on average). The transparent transistors were further utilized to construct a fully transparent and flexible logic inverter on a plastic substrate and also used to control commercial GaN light-emitting diodes (LEDs) with light intensity modulation of 10^3. Our results suggest that aligned nanotubes have great potential to work as building blocks for future transparent electronics.

KEYWORDS: transparent transistor · flexible transistor · aligned nanotube · transfer printing · transparent display

Transparent electronics (also called invisible electronics)[1] acting as an emerging technology for the next generation of optoelectronic devices has attracted numerous research efforts in recent years due to its great potential to make significant commercial impact in a wide variety of areas.[2−8] Central to the realization of transparent electronics is the development of transparent thin-film transistors (TTFTs), the key performance metrics of which would be high device mobility and low-temperature fabrication. Generally, high device mobility enables fast device operation and low power consumption, which broadens the application area of TTFTs. On the other hand, low-temperature fabrication is essential for transparent devices made on flexible substrates, which would enable novel applications such as e-paper, wearable display, smart tag, and artificial skin (E-skin).[9−11] Low-temperature fabrication of TTFTs also lowers the fabrication expense significantly.[12−14]

Traditionally, wide band gap semiconductors were studied for TTFTs, such as GaN and oxide semiconductor films.[2,3,7,15−17] However, TTFTs fabricated in these cases usually exhibit rather moderate mobilities. For instance, TTFTs fabricated using In−Ga−Zn−O film only have device mobility of ~80 and ~9 $cm^2 V^{-1} s^{-1}$ on glass and polyethylene terephthalate (PET) substrates, respectively.[2,3] TTFTs with In_2O_3 films coupled with an organic dielectric layer exhibited mobility of 120 $cm^2 V^{-1} s^{-1}$ on glass substrates.[7] Recently, semiconductor nanowires have emerged as another class of materials that can be used to fabricate TTFTs,[8,18] and our research group has developed transparent transistors using In_2O_3 nanowires with a mobility of 514 $cm^2 V^{-1} s^{-1}$.[8]

Despite the above-mentioned success, the reported mobility values are still low compared to those of nontransparent devices, indicating further room for improvement. In addition, those oxide-based TTFTs were limited to n-type transistors,[2,3,6−8,16,18] and the development of high-performance transparent p-type transistors, which is an essential element in CMOS, still remains a great challenge.

To realize high-performance p-type TTFTs with high mobility, single-walled carbon nanotubes (SWNTs) can be a promising candidate for their intrinsic mobility over 100 000 $cm^2 V^{-1} s^{-1}$,[19] good mechanical flexibility,[20] and good optical transparency.[4,5,21] In addition, carbon nanotube devices usually exhibit p-type transport behavior,[22,23] which complements the

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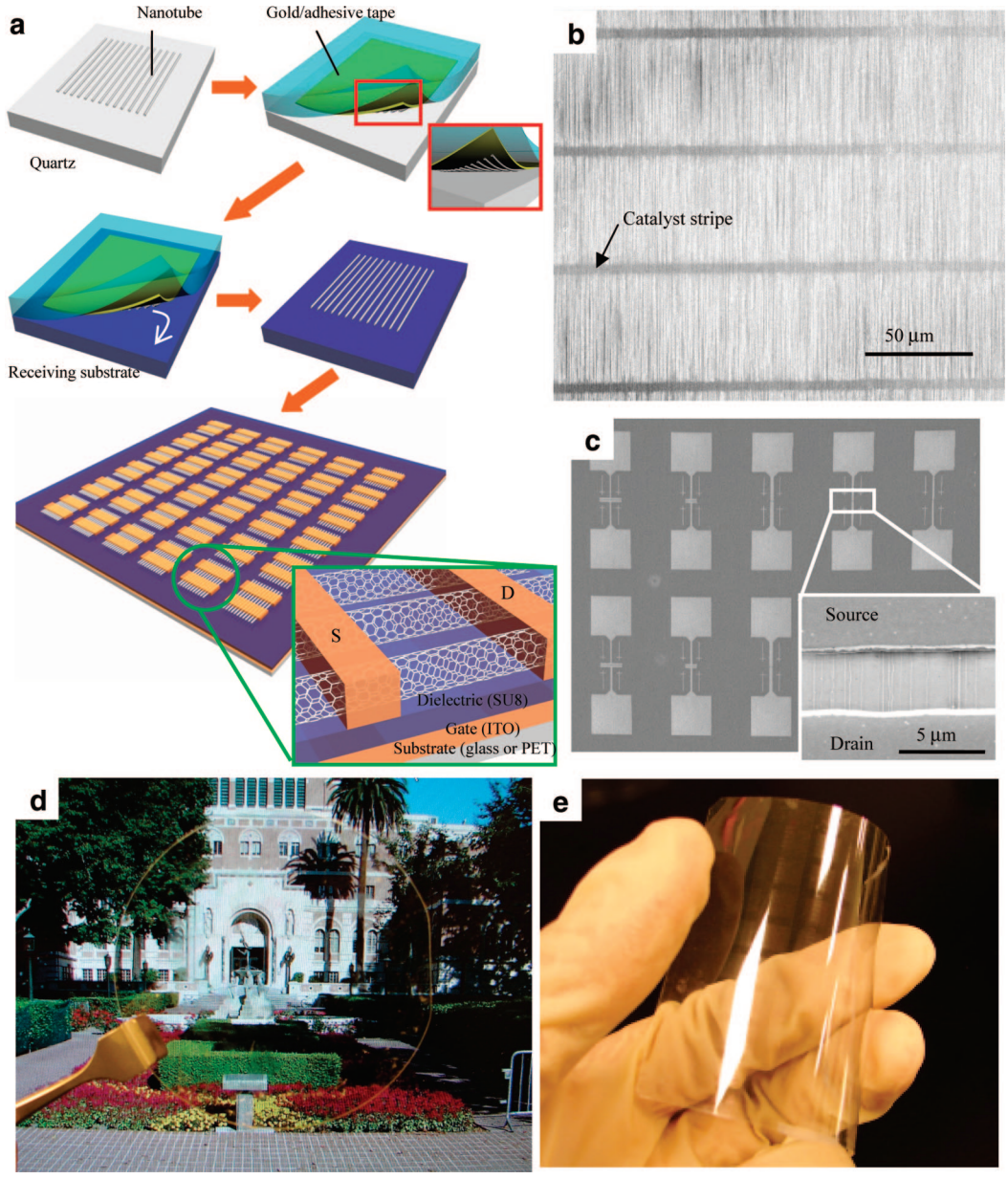

Figure 1. Fabrication of fully transparent aligned SWNT transistors. (a) Schematic diagram of aligned SWNT transfer and a device structure consisting of a substrate (glass or PET), ITO as back gate, SU8 as dielectric, aligned SWNTs as channel, and ITO as source and drain. (b) SEM image of transferred aligned SWNTs on SU8 on a glass substrate. (c) SEM image of devices showing the ITO source and drain electrodes fabricated on glass. Inset: SEM image of aligned nanotubes bridging ITO electrodes. (d) Optical micrograph of fully transparent aligned SWNT transistors on a 4 in. glass wafer. (e) Optical micrograph of fully transparent aligned SWNT transistors on a PET sheet of 3 in. × 4 in.

n-type oxide-based TTFTs. In recent years, random nanotube networks were used as active channels for TTFTs,[4,5,21] but the best obtained mobility was ~30 $cm^2 V^{-1} s^{-1}$.[5] This low mobility might result from the fact that electrical conduction in a random nanotube network has to go through many nanotube−nanotube junctions. Aligned carbon nanotubes which can directly bridge source and drain are therefore expected to offer better performance.

In this work, we have achieved both high mobility and low-temperature processing for TTFTs made with highly aligned single-walled carbon nanotubes. These nanotubes were first grown on quartz substrates and then transferred to glass or PET substrates with prepatterned indium−tin oxide (ITO) gate electrodes, followed by patterning of transparent source and drain electrodes. In contrast to random networked nanotubes, the use of massively aligned nanotubes enabled the devices to exhibit high performance, including high mobility, good transparency, and mechanical flexibility. In addition, these aligned nanotube transistors are easy to fabricate and integrate, as compared to individual nanotube devices. The transfer printing process allowed the devices to be fabricated through low-temperature process, which is particularly important for realizing transparent electronics on flexible sub-

strates. We first demonstrated fully transparent high mobility (1300 $cm^2 V^{-1} s^{-1}$) p-type transistors on glass substrates with transparency of about 80% in the visible light regime. Transparent devices with high on/off ratio (3×10^4) were then realized through electrical breakdown. Fully transparent and mechanically flexible devices were also fabricated on PET substrates, with a transparency of 80%. Flexible PMOS inverters with a gain of ~0.38 with $V_{DD} = 5$ V were successfully fabricated on flexible PET substrates. In addition, fully transparent aligned nanotube devices were used to control commercial GaN LED with an on/off ratio of 10^3 in the light intensity.

RESULTS AND DISCUSSION

Fabrication of Transparent Aligned Nanotube Transistors on Glass and PET. Figure 1a shows a schematic diagram of our transfer printing method and the structure of the transparent transistors. The aligned nanotubes were first grown on quartz substrates using chemical vapor deposition (CVD).[24,25] The transfer started by coating as-grown aligned SWNTs on a quartz substrate with a 100 nm thick Au film. Revalpha thermal tape (from Nitto Denko), which is adhesive at room temperature but loses adhesion above 120 °C, was placed on the Au film and then peeled off slowly that resulted in picking up the nanotube/Au film. The thermal tape/Au film/aligned SWNT film was placed onto a target substrate with an ITO back gate and a SU8 dielectric layer, and the whole structure was heated up to 130 °C on a hot place to detach the thermal tape. The Au film was removed by a gold etchant, leaving the aligned SWNTs on the target substrate. Finally, source and drain electrodes made of thin layer of Au plus ITO or ITO only were defined by photolithography and lift-off techniques as described in the Methods section. The thin layer of Au was used to reduce the contact resistance, as shown later. The printing transfer method allowed the construction of devices on any substrates including glass and PET, and a device yield as high as 100% was accomplished easily due to high coverage of the substrates with the aligned SWNTs. Shown in Figure 1b is a representative scanning electron microscopy (SEM) image of transfer aligned SWNTs on a glass substrate covered with SU8. These nanotubes are typically more than 50 μm in length and 1−2 nm in diameter with a density of 2−3 tubes per micron, and most of the nanotubes can directly bridge the source and drain for a majority of the device dimensions studied. Figure 1c is a SEM image of the devices with different channel widths from 8 to 100 μm. The channel length keeps at 4 μm. The inset in Figure 1c is a typical SEM image of the aligned SWNTs between source and drain, showing the nanotubes remain highly ordered after the whole fabrication process. Figure 1d,e depicts the optical micrographs of devices fabricated on a 4 in. glass wafer and a piece of PET sheet, respectively. They show clear good transparency, as the backgrounds can be easily seen through these devices.

Performance of Aligned SWNT TTFTs on Glass. Figure 2a shows the schematic diagram of the transparent device on glass, with an inset of an optical micrograph of a glass substrate with an array of devices in the highlighted region. These transistors have aligned nanotubes as the active channel with a channel width of 10, 20, 50, 100, and 200 μm and a channel length of 4, 10, 20, 50, and 100 μm. We used the ITO film on glass as the back gate, 2 μm thick SU8 as the gate dielectric, and two kinds of source/drain contact materials: 1 nm Au/100 nm ITO and 100 nm ITO. The transparency of the devices was measured, and the results are shown in Figure 2b, which revealed that the devices with Au/ITO contacts had a transmittance of ~80% in the visible light regime (400−800 nm). Compared with the devices using only ITO as the contacts, the transmittance decreased about 5% due to the thin Au layer. The performance of our devices was then characterized. Figure 2c,d shows representative plots of drain−source current (I_{ds}) *versus* drain−source voltage (V_{ds}) and I_{ds} *versus* gate voltage (V_g), respectively, for a device with a channel length of 50 μm and a width of 100 μm. The nanotube density was measured to be 2−3 aligned SWNTs per micron. The device showed p-type transistor behavior and an on/off ratio of ~20 due to the presence of metallic nanotubes. The large operation voltage (gate voltage) can be reduced by employing thin and/or high-k dielectrics, such as HfO_2 or self-assembled organic nanodielectrics.[7] Figure 2e gives a typical $I_{ds}-V_g$ plot and the extracted transconductance (dI_{ds}/dV_g) at $V_{ds} = 1$ V, showing a peak value of 1.2 μA/V. The transconductance can be easily improved by utilizing higher capacitance dielectrics, such as high-k dielectrics. The effective mobility (μ) of the devices was calculated from the maximum transconductance by applying the following equations.[24]

$$\mu = \frac{L}{V_d C_W W} \cdot \frac{dI_d}{dV_g}$$

where L is the channel length, and W is the channel width. C_W is the specific capacitance per unit area of the aligned nanotube channel calculated as follows[24]

$$C_W = \frac{D}{\left[C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_S} \cdot \log\left[\frac{\sin h(2\pi tD)}{\pi RD}\right]\right]}$$

where D is the density of nanotubes, C_Q is the quantum capacitance of nanotubes, t is the thickness of the dielectric layer, R is the radius of nanotubes, and ϵ_S is the dielectric constant at the interface where the nanotubes are placed. For our case, ϵ_S was estimated to be ~2 since we had air/SWNT/SU8 structure. The value of C_Q was taken from a previous report.[26] Figure 2f shows

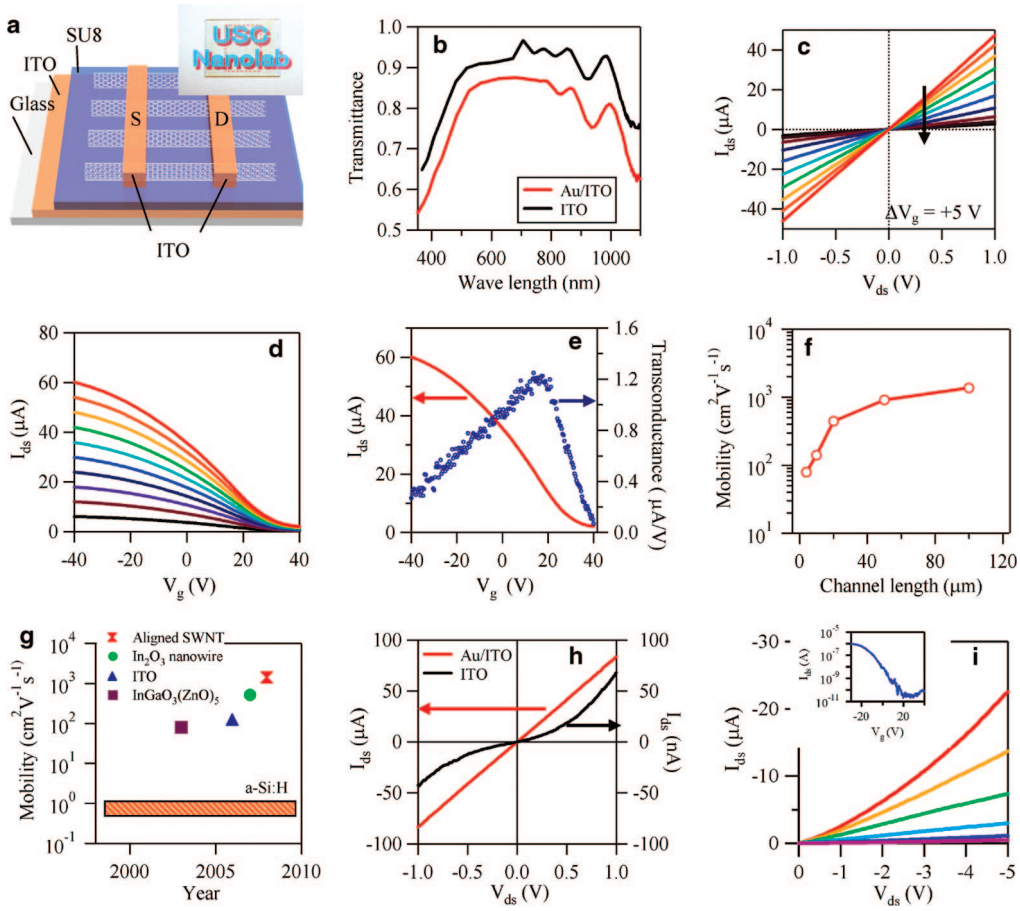

Figure 2. High mobility transparent aligned SWNT transistors on glass. (a) Schematic diagram of a fully transparent aligned SWNT transistor. Inset shows an optical micrograph of a glass substrate with arrays of transparent aligned SWNT transistors. (b) Optical transmittance of glass substrates with arrays of transparent aligned SWNT transistors with Au/ITO (red curve) and ITO (black curve) contacts. (c) $I_{ds}-V_{ds}$ curves of a 100 μm wide and 50 μm long aligned SWNT transistor with Au/ITO contact under different V_g from −20 (red curve) to 20 V (black curve) with a step of 5 V. (d) $I_{ds}-V_g$ curves of the same device under different V_{ds} from 0.1 to 1.0 V (the step of V_{ds} was 0.1 V). (e) Plots of I_{ds} and transconductance *versus* V_g for the same device. (f) Mobility *versus* channel length for aligned SWNT transistors with Au/ITO contacts. The channel width of all the devices was 200 μm. (g) Plot of the mobilities of transparent transistors reported in the literature, with carrier mobilities for a-Si:H thin-film transistors also shown. (h) Typical $I_{ds}-V_{ds}$ plots for devices Au/ITO (red) and ITO (black) contacts under V_g = 0 V, respectively. (i) $I_{ds}-V_{ds}$ curves of an aligned SWNT transistor with ITO contacts showing high on/off ratio. V_g varied from −10 (red curve) to 10 V (black curve) at a step of 5 V. Inset shows an $I_{ds}-V_g$ curve of the same device in log scale with V_{ds} =0.5 V.

the mobility plotted against channel length, and an effective mobility of 1300 $cm^2\ V^{-1}\ s^{-1}$ was realized for the devices with a channel length of 100 μm. This mobility is the highest one among the transparent transistors using various active materials reported so far.[3−8,16−18,21] Similar mobility and transconductance were observed for devices with similar dimensions. The variation of the mobility and transconductance was within ∼30%, indicating the uniformity of the aligned nanotube network. Channel length-dependent mobility was clearly observed, indicating the presence of small Schottky barriers between the carbon nanotubes and the Au/ITO contacts.[24] As a reference, Figure 2b summarizes the mobility of representative transparent devices reported in recent years and amorphous silicon (a-Si:H). One can see that aligned nanotubes offer much higher mobility than competing materials, such as In_2O_3 nanowires (∼514 $cm^2\ V^{-1}\ s^{-1}$),[8] In_2O_3 films (∼120 $cm^2\ V^{-1}\ s^{-1}$),[7] and $InGaO_3(ZnO)_5$ films (∼80 $cm^2\ V^{-1}\ s^{-1}$).[2] The high mobility of aligned nanotube devices would enable low operation voltage, low power consumption, and high switching speed, which are attractive for several applications such as transparent circuits in portable displays. This high mobility was realized by our careful study of the effect of contact materials on the device performance. Devices using different contacts were also fabricated, and Figure 2h shows the I_{ds} *versus* V_{ds} plots for two devices with Au/ITO (red curve) and ITO only contact (black curve). It was found that the devices with a thin Au layer exhibited larger conductance by about 3 orders of magnitude than those without Au. We attribute this difference in conductance to the difference in work functions for gold and ITO, which are 5.3[27] and 3.9−4.4 eV,[28] respectively. Compared with the nanotube work function (4.7−5.1 eV[29,30]), we expect gold can form rather ohmic

contacts to nanotubes, while ITO would present a Schottky barrier at contacts. This is also consistent with the observation that the Au/ITO contacts led to a linear $I_{ds}-V_{ds}$ curve, while the ITO contact yielded nonlinear $I_{ds}-V_{ds}$ curve (Figure 2h). We note this is the first report of using a thin layer of gold to reduce the Schottky barrier between ITO and nanotubes for transparent electronics.

Improvement of the on/off ratio for the transparent aligned nanotubes devices can be further achieved with electrical breakdown to remove metallic carbon nanotubes. During the breakdown process, V_{ds} was increased gradually while the V_g was kept constant at a high positive value (20 V). Figure 2i shows a family of $I_{ds}-V_{ds}$ curves of a device after breakdown. Gate voltages with steps of 5 V were applied. The results indicate good gate dependence and on/off ratio with clearly separated curves. We note that electrical breakdown led to lower effective device mobility, as inevitably some semiconductive nanotubes were also damaged due to the high V_{ds} applied during breakdown. For typical devices, the mobility decreased from ~1300 $cm^2 V^{-1} s^{-1}$ before breakdown to 700−800 $cm^2 V^{-1} s^{-1}$ after breakdown when the on/off ratio was increased by a factor of 2.5. For the device, an output current of ~−23 μA was obtained at $V_{ds} = -5$ V under $V_g = -10$ V, revealing device resistance of ~220 kΩ. The inset of Figure 2i is the $I_{ds}-V_g$ curve in log scale with $V_{ds} = 0.5$ V, showing an on/off ratio of 3×10^4.

Performance of Aligned SWNT TTFTs on PET. Fully transparent and flexible aligned SWNT devices using PET substrates were also fabricated with ITO back gate, 2 μm thick SU8 as the gate dielectric, and ITO as source and drain (Figure 1a). Electronic devices on flexible substrates are extremely attractive owing to the proliferation of wearable, hand-held, portable consumer electronics as well as the compatibility with roll-to-roll fabrication.[9,11,13,14,31] Figure 3a is the transmittance of the transparent and flexible devices. The optical transmission is ~80% in the 350−1200 nm wavelength range. The inset in Figure 3a is an optical micrograph of devices on a piece of PET sheet. To evaluate the flexibility of our devices, $I_{ds}-V_g$ measurements were performed under bending of the substrates with different angles, and the plots are shown in Figure 3b. The $I_{ds}-V_g$ curves correspond to a device bended for 0 (purple), 30 (blue), 60 (light blue), 90 (yellow), and 120° (red), respectively, with a channel length of 10 μm and a width of 200 μm. The inset in Figure 3b shows a picture of the bending experimental setup, with the bending angle defined as 180° − θ. The transconductance and on current of the device at each bending angle were extracted from these curves and were plotted in Figure 3c. One can see that the device continued to perform for bending angles from 0 to 120°, and the variation for both the transconductance and the on current were rather small. Furthermore, the device was successfully

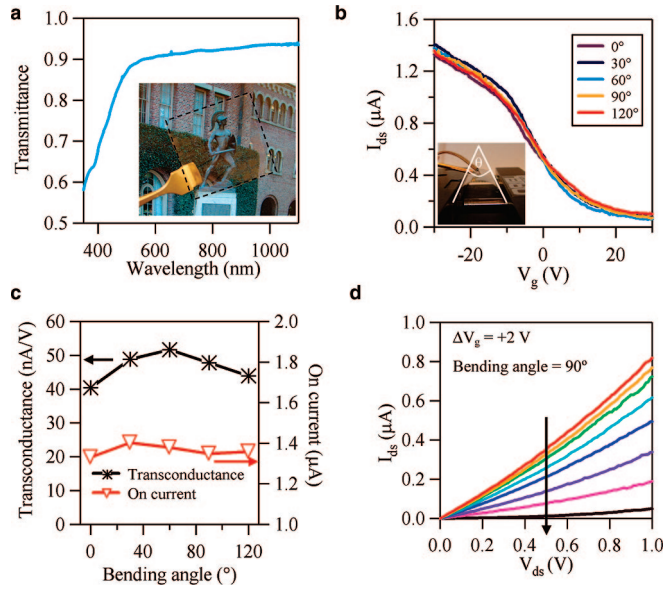

Figure 3. Fully transparent and flexible aligned SWNT transistors on PET substrates. (a) Optical transmittance of a PET substrate with arrays of transparent aligned SWNT transistors with ITO contacts. Inset is an optical micrograph of a piece of PET sheet with aligned nanotube TTFTs. (b) $I_{ds}-V_g$ curves of a representative device under different bending angles. Inset shows an optical micrograph of the experimental setup to measure $I_{ds}-V_g$ under bending of the substrate. (c) On current (red) and transconductance (black) extracted from the data in Figure 3b *versus* bending angle. (d) $I_{ds}-V_{ds}$ curves of a fully transparent flexible aligned SWNT transistor under different V_g with bending of the substrate by 90°. V_g was swept from 6 (red curve) to 20 V (black curve) with a step of 2 V.

operated as a transistor on a bended substrate as shown in Figure 3d, where $I_{ds}-V_{ds}$ curves at different V_g were plotted. As a whole, these data represent that aligned nanotube transparent transistors were successfully fabricated on PET substrates with good mechanical flexibility. The comparatively low transconductance of these devices resulted from the fact that only ITO was used to contact the nanotubes for high transparency. In case high transconductance is needed for such flexible transparent devices, one can improve the transconductance easily by depositing a thin Au layer between SWNTs and ITO, as demonstrated above.

Fully Transparent PMOS Inverters and LED Driving Circuitry. Our ability to fabricate high-performance transparent and flexible transistors enabled us to apply them toward transparent circuits and transparent displays. Figure 4a shows an optical micrograph of fully transparent and flexible PMOS logic gates (inverters) on PET using transfer printed aligned SWNTs. The inset is the circuit diagram of the inverter, where one aligned SWNT transistor with an individually addressable gate was used as the drive and another transistor with another individual back gate fixed at $V_g = 0$ V as the load. The output voltage (V_{out}) of the inverter was plotted *versus* V_{in} in Figure 4b, together with the gain defined as dV_{out}/dV_{in}. A maximum gain of ~0.38 was obtained at $V_{in} = -12$ V. This inverter gain is largely a consequence of the polymer dielectric used and can be improved by using

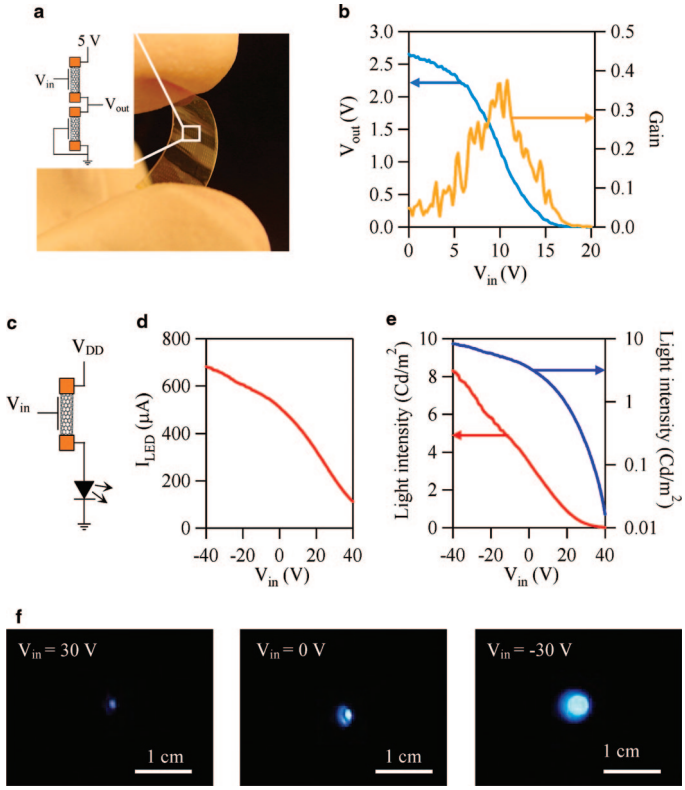

Figure 4. Application of fully transparent SWNT transistors for a PMOS inverter and LED driving circuitry. (a) Optical micrograph of fully transparent logic gates (inverters) on PET. The inset shows the circuit diagram of the PMOS inverter. (b) Plots of V_{out} (blue) and inverter gain (yellow, defined as dV_{out}/dV_{in}) *versus* V_{in} of a fully transparent flexible PMOS inverter. (c) The circuit diagram of a LED driven by a transparent SWNT transistor. (d) Plot of the output current through the LED (I_{LED}) *versus* V_{in} with $V_{DD} = 9$ V. (e) LED light intensity *versus* V_{in} in linear (red) and log (blue) scale, respectively, with $V_{DD} = 9$ V. (f) Optical images of the LED under $V_{in} = 30$, 0, and -30 V.

better dielectrics, such as high-k dielectric and/or thinner dielectric materials.

Finally, we have studied using the aligned nanotubes transparent transistors to control various light-emitting devices as a proof-of-concept for future transparent displays. A GaN LED was selected for the proof-of-concept study and was wire-bonded on a breadboard together with an aligned nanotube transparent chip. Figure 4c shows the circuit diagram of the experiment, where one TTFT was connected to LED, and V_{DD} was applied to the drain of the transistor. By controlling V_{in} that worked as gate voltage for the transistor with fixed V_{DD}, we have controlled the voltage drop across the LED. Figure 4d shows the current flowing through the LED, which was successfully modulated by V_{in} by a factor of ~7. This modulation led to control of the LED light intensity as shown in Figure 4e, where the light intensity was plotted against V_{in} in linear (red curve) and in log (blue curve) scale, respectively. The ratio of the light intensity at the off state and on state reached $\sim 10^3$. Figure 4f shows photographs of the LED operated with $V_{in} = 30$ (left), 0 (middle), -30 (right) V, respectively, clearly showing the significant light intensity modulation.

In summary, we have demonstrated the great potential of massively aligned single-walled carbon nanotubes for high-performance transparent electronics. These aligned nanotube transistors with transparent contacts showed good transparency and very high mobility and can be made compatible with both rigid and flexible substrates due to the low-temperature processing employed. We achieved device mobility as high as 1300 $cm^2 V^{-1} s^{-1}$ on glass substrates, which is the highest among transparent transistors reported so far. Electrical breakdown was then utilized to obtain high on/off ratios ($\sim 3 \times 10^4$). Fully transparent and flexible transistors were also fabricated, showing very good mechanical flexibility for bending up to 120°. The transparent transistors were further utilized to construct a fully transparent and flexible logic inverter on a plastic substrate and also used to control commercial GaN light-emitting diodes with light intensity modulation of 10^3. While large manufacturability must be addressed before practical applications are considered, our work has paved the way for using aligned nanotubes for high-performance transparent electronics.

METHOD

Device Fabrication. Aligned SWNTs were grown using chemical vapor deposition at 900 °C with a gas flow of 2500 sccm CH_4, 10 sccm C_2H_4, and 600 sccm H_2. As-grown nanotubes were coated with 100 nm gold film evaporated by an e-beam evaporator. Gold-coated nanotubes were picked up by pressing a piece of Revalpha tape (#3198M from Nitto Denko) against the sample and then peeling off slowly. Before transferring the nanotubes, glass substrates were prepared with a common ITO (100 nm) back gate, while PET substrates were prepared with individual back gates made by photolithography, ITO sputtering, and lift off. SU8 2002 (2 μm in thickness) was then spin-coated onto both substrates and cured. Transfer started with pressing the thermal tape with gold film and nanotubes against a target substrate. The target substrate was then heated up to 130 °C, which resulted in loss of adhesion of the thermal tape to remove the tape while leaving the gold film with nanotubes on the target substrate. As the final step of the transfer, the gold film was removed by gold etchant (KI/I_2). Following the transfer, photolithography was used to define openings for source and drain electrodes. For some devices, gold (1 nm) was then evaporated using an e-beam evaporator followed by sputtering of ITO (100 nm) to form the contacts. Some other devices only had ITO as the contact electrodes with the goal of studying the effect of contact materials. Finally, photolithography was again used to mask the channel regions with a photoresist, followed by oxygen plasma treatment to etch unwanted carbon nanotubes outside the channels.

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Supporting Information Available: Additional information on multiple transfer of aligned carbon nanotubes, histogram of the on/off ratio before and after electrical breakdown, analysis of

square resistance and contact resistance, and transparent n-type transistor by PEI coating. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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